Karnataka State Council for Science and Technology

Indian Institute of science, Bangalore-560012

KSCST

36th series of Student Projects Programme (Engineering)

A Report on

A Low power content addressable memory for networking applications

Submitted in fulfillment of the requirement for the 36th series of SPP and award of the degree of

BACHELOR OF ENGINEERING

in

ELECTRONICS AND COMMUNICATION

By

Roshan Gururmurthy (1PI09EC093)

Rueju N (1PI09EC095)

Varun R (1PI09EC0123)

Under the Guidance of

Prof. Geetha Prakash

Dept. of ECE., PESIT

Bangalore 560 085

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

P.E.S. INSTITUTE OF TECHNOLOGY

(An Autonomous Institute Under VTU, Belgaum)

BANGALORE 560085

2012 – 2013

ABSTRACT

Content addressable memories (CAMs) are widely used in the network applications, such as flow analysis and classless inter-domain routing. In comparison with the random access memory (RAM), however, high power dissipation is one of major disadvantages of the CAM. Effective power-reduction techniques thus are very important for designing a CAM.

In This Project we aim:

I. To design (ASIC flow) a CAM macros for IPV6 lookup table, which achieves significant reduction in power as compared to:

- Conventional NOR- type CAM
- Conventional NAND-NOR type Hybrid CAM,

without much sacrifice in delay or transistor count.

Simulation tool: Cadence Virtuoso 6.1.4 version.

Technology: 180nm.

II. To implement the developed scheme (at an algorithmic level) on a Verilog test bench.

Software: Xilinx v12.1.