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A PROJECT REPORT

ON

HIGH SPEED FPGA DESIGN FOR SIMPLE MULTIPLIER USING VEDIC MATHEMATICS

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ABSTRACT

For arithmetic multiplication Vedic multiplication techniques Urdhva tiryakbhyam has been thoroughly discussed. It has been found that Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay for multiplication of all types of numbers, either small or large. It literally means "Vertically and crosswise". Further 4x4 bits, 8x8 bits and 16x16 bits multiplication has been designed. Here we have used vedic multiplication to reduce the power consumption and delay. This method of multiplication helps to get the product much faster. Here multiplier of n bit size has n2 gates. Here we are implementing the circuit using FPGA by Xilinx Synthesis Tool on Spartan 3E kit. Here we can also find the design for 32x32 bits and 64x64 bits using the same technique. Here we have also got the hardware implementation for this. The same method can be used to find the square of the number. We are trying to implement using the verilog program.