

PROJECT REPORT ON
NEW HIGH-SPEED CMOS FULL ADDER CELL OF MIRROR
DESIGN STYLE

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ABSTRACT

The era of the age brings about faster more miniature and efficient computing system to the consumer. The world run on this constant battle of the design matrices of low power and miniaturization to optimize computing speed. One of the basic element of any computing system is the adder. A crucial fast adder is the need of any system that is part of this technological era.

A new circuit of a high-speed CMOS full adder cell is presented. The proposed adder cell refers to the CMOS adders class executed on CMOS mirror design style, with the attributes intrinsic to this class: absence of power consumption in a static mode, absence of incomplete levels of voltages inside the circuit and, hence, necessity to restore these levels. The proposed solution of adder cell provides a higher speed of carry signal formation as compared to the known adders and, hence, allows achieving high speed of the N-bit adder device. The proposed cell has been compared to the other three basic cells.