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A PROJECT REPORT ON

**“Dynamic Domino Logic Circuits Design for
Low Power VLSI Design”**

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ABSTRACT

Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favored in high performance designs because of the speed advantage offered over static CMOS logic circuits. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power dissipation. In this work, a new reduced-swing domino logic technique is presented which provides significantly lower power dissipation as compared to traditional domino circuit structures. Additionally, the noise margins of the new circuit offer an improvement over standard domino design.

The key idea of the new design style is to limit both the upper and lower bounds of the voltage swing at the internal dynamic node. The voltage swing at the inputs and the outputs of the domino circuit remains full-swing. A number of circuits are presented all of which have been designed and simulated in 0.18 micron technology. Analysis of simulation results shows the potential for a decrease in power consumption with an increased tolerance to noise. These improvements come at the expense of increased propagation delay and circuit area; the magnitude of which varies with the proposed circuit structures. The design styles are compared by performing detailed transistor level simulations on benchmark circuits such as OR2 gate, AND2 gate and 16:1 MULTIPLEXER.