PROJECT REPORT ON

SRAM WITH MEMORY REDUNDANCY

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As prescribed by Visvesvaraya Technological University in partial fulfilment of the requirements for the award of degree of

BACHELOR OF ENGINEERING

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

Under the guidance of

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Near Mangalore University, MANGALORE-574153, KARNATAKA

2010-2011

ABSTRACT

ELECTRONICS is a branch of science and technology which deals with generation, distribution, switching, conversion and **storage.** Each process and procedure yields useful result which can be used for further enhancement and improvement in the result with updating technology. This can be enabled only if the results are stored and hence the storage is the basic requirement in the analog and digital domain. MEMORY is the basic element used for storage. With the increase in the technology usage, there is an instantaneous decrease in the chip size and hence the memory required should also be miniaturized. This is the main reason for the evolution of memories like SRAM,DRAM etc.

SRAM is used in applications where the data efficiency is critical factor. In particular it can be considered to be improved version of DRAM, capacitor being replaced by gate capacitances of MOSFETS and refresh circuit provided by cross coupled inverters. There are some digital circuits wherein the throughput and cost are also the key factors with the data efficiency. In such cases the SRAM will be connected with extra memory columns/rows which are used in place of the corrupted columns/rows.

The corrupted bit in a SRAM array may be the reason for replacement of the entire memory array, which makes the SRAM arrays costly. Our project aims at replacement of the column containing the corrupted bit, with a new column. So the SRAM array contains one or more redundant columns with the supporting blocks.